What is claimed is:

1. A liquid crystal display comprising:

a first panel including a common electrode extending in a horizontal direction along a surface of the first panel; and

a second panel connected to the first panel and spaced from the first panel, the second panel including a pad extending in the horizontal direction along a surface of the second panel, the pad being spaced from the common electrode in the horizontal direction.

2. The liquid crystal display according to claim 1, wherein the pad is a gate pad.

3. The liquid crystal display according to claim 1, wherein the pad is a source pad.

4. The liquid crystal display according to claim 1, wherein the common electrode extends along an entire horizontal surface of the first panel.

5. The liquid crystal display according to claim 1, wherein the pad is spaced from an edge of the first panel in the horizontal direction, wherein the edge of the first panel is the edge of the first panel that is located closest to the pad.

6. The liquid crystal display according to claim 1, wherein said common electrode is made of Indium Tin Oxide.

7. The liquid crystal display according to claim 1, further comprising a passivation layer on the second panel and a cut protection member is provided on the second panel for protecting the passivation layer during a cutting process of the LCD.

8. The liquid crystal display according to claim 7, wherein the cut protection member is made of Indium Tin Oxide.

9. The liquid crystal display according to claim 1, wherein the pad is a gate pad, the liquid crystal display further comprising a gate bus line connected to the gate pad, a source pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

10. The liquid crystal display according to claim 1, wherein the pad is a source pad, the liquid crystal display further comprising a gate pad, a gate bus line connected to the gate pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

11. A liquid crystal display comprising:

a first panel including a common electrode extending in a horizontal direction along a surface of the first panel; and

a second panel connected to the first panel and spaced from the first panel, the second panel including a pad terminal extending in the horizontal direction along a surface of the second panel, the pad terminal being spaced from the common electrode in the horizontal direction.

12. The liquid crystal display according to claim 11, wherein the pad terminal is a gate pad terminal.

13. The liquid crystal display according to claim 11, wherein the pad terminal is a source pad terminal.

14. The liquid crystal display according to claim 11, wherein the common electrode extends along an entire horizontal surface of the first panel.

15. The liquid crystal display according to claim 11, wherein the pad terminal is spaced from an edge of the first panel in the horizontal direction, wherein the edge of the first panel is the edge of the first panel that is located closest to the pad terminal.

16. The liquid crystal display according to claim 11, wherein said common electrode and said pad terminal are made of Indium Tin Oxide.

17. The liquid crystal display according to claim 11, further comprising a passivation layer on the second panel and a cut protection member is provided on the second panel for protecting the passivation layer during a cutting process of the LCD.

18. The liquid crystal display according to claim 17, wherein the cut protection member is made of Indium Tin Oxide.

19. The liquid crystal display according to claim 11, wherein the pad is a gate pad, the liquid crystal display further comprising a gate bus line connected to the gate pad, a source pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

20. The liquid crystal display according to claim 11, wherein the pad is a source pad, the liquid crystal display further comprising a gate pad, a gate bus line connected to the gate pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

Subst. A3

21. A liquid crystal display comprising:

a first panel including a first ITO layer extending in a horizontal direction along a surface of the first panel; and

a second panel connected to the first panel and spaced from the first panel, the second panel including a second ITO layer extending in the horizontal direction along a surface of the second panel, the second ITO layer being spaced from the first ITO layer in the horizontal direction.

22. The liquid crystal display according to claim 21, wherein the first ITO layer is a common electrode and the second ITO layer is a pad terminal.

23. The liquid crystal display according to claim 22, wherein the pad terminal is a gate pad terminal.

24. The liquid crystal display according to claim 22, wherein the pad terminal is a source pad terminal.

25. The liquid crystal display according to claim 22, wherein the common electrode extends along an entire horizontal surface of the first panel.

26. The liquid crystal display according to claim 22, wherein the second ITO layer is spaced from an edge of the first panel in the horizontal direction, wherein the edge of the first panel is the edge of the first panel that is located closest to the second ITO layer.

27. The liquid crystal display according to claim 22, further comprising a passivation layer on the second panel and a cut protection

member is provided on the second panel for protecting the passivation layer during a cutting process of the LCD.

28. The liquid crystal display according to claim 27, wherein the cut protection member is made of Indium Tin Oxide.

29. The liquid crystal display according to claim 21, further comprising a gate pad, a gate bus line connected to the gate pad, a source pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

30. The liquid crystal display according to claim 29, further comprising a gate pad, a gate bus line connected to the gate pad, a source pad, a source bus line connected to the source pad, a thin film transistor having a gate electrode extending from the gate bus line, a source electrode extending from the source bus line, a drain electrode facing the source electrode and a pixel electrode connected to the drain electrode.

31. A method for manufacturing a liquid crystal display comprising steps of:

forming a first panel including a common electrode;

forming a second panel including a pad;

joining the first panel and the second panel together such that the first panel is spaced from the second panel;

inserting a liquid crystal between the first panel and the second panel; and

cutting a portion of the first panel covering the pad in order to expose the pad so that the pad does not overlap with the common electrode.

32. The method according to claim 31, wherein the common electrode is formed along an entire horizontal surface of the first panel.

33. The method according to claim 31, wherein the pad is a gate pad.

34. The method according to claim 31, wherein the pad is a source pad.

35. The method according to claim 31, further comprising the step of forming a cut protection member on the second panel for protecting the liquid crystal display during the cutting step.

36. The method of claim 31, wherein after the cutting step, the pad is spaced apart from an edge of the first panel in a horizontal direction, the edge of the first panel being the edge of the first panel that is located closest to the pad.

37. The method according to claim 31, wherein the pad is a gate pad, the method further comprising the steps of forming a gate bus line connected to the gate pad, forming a source pad, forming a source bus line connected to the source pad, forming a thin film transistor having a gate electrode extending from the gate bus line, forming a source electrode extending from the source bus line, forming a drain electrode facing the source electrode and forming a pixel electrode connected to the drain electrode.

38. The method according to claim 31, wherein the pad is a source pad, the method further comprising the steps of forming a gate pad, forming a gate bus line connected to the gate pad, forming a source bus line connected to the source pad, forming a thin film transistor having a gate electrode extending from the gate bus line, forming a source electrode extending from the source bus line, forming a drain electrode facing the source electrode and forming a pixel electrode connected to the drain electrode.

39. A method for manufacturing a liquid crystal display comprising steps of:

forming a first panel including a common electrode;

forming a second panel including a pad terminal;

joining the first panel and the second panel together such that the first panel is spaced from the second panel;

inserting a liquid crystal between the first panel and the second panel; and

cutting a portion of the first panel covering the pad terminal in order to expose the pad terminal so that the pad terminal does not overlap with the common electrode.

40. The method according to claim 39, wherein the common electrode is formed along an entire horizontal surface of the first panel.

41. The method according to claim 39, wherein the pad terminal is a gate pad terminal.

42. The method according to claim 39, wherein the pad terminal is a source pad terminal.

43. The method according to claim 39, further comprising the step of forming a cut protection member on the second panel for protecting the liquid crystal display during the cutting step.

44. The method of claim 39, wherein after the cutting step, the pad terminal is spaced apart from an edge of the first panel in a horizontal direction, the edge of the first panel being the edge of the first panel that is located closest to the pad terminal.

45. A method for manufacturing a liquid crystal display comprising steps of:

forming a first ITO layer on a first panel;

forming a second ITO layer on a second panel;

joining the first panel and the second panel together such that the first panel is spaced from the second panel;

inserting a liquid crystal between the first panel and the second panel; and

cutting a portion of the first panel covering the second ITO layer on the second panel so that the first and second ITO layers do not overlap with each other.

46. The method according to claim 45, wherein the first ITO layer defines a common electrode.

47. The method according to claim 46, wherein the common electrode is formed along an entire horizontal surface of the first panel.

48. The method according to claim 45, wherein the second ITO layer defines a gate pad terminal.

49. The method according to claim 45, wherein the second ITO layer defines a source pad terminal.

50. The method according to claim 45, further comprising the step of forming a cut protection member on the second panel for protecting the liquid crystal display during the cutting step.

51. The method according to claim 50, wherein the cut protection member is formed of the second ITO layer on the second panel.

52. The method of claim 45, wherein after the cutting step, the second ITO layer is spaced apart from an edge of the first panel in a horizontal direction, the edge of the first panel being the edge of the first panel that is located closest to the second ITO layer.